ANALYSIS, DESIGN AND IMPLEMENTATION OF MICROCONTROLLER BASED VARIABLE LOW FREQUENCY 3-PHASE POWER SUPPLY

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CHAPTER 1

INTRODUCTION

 ► Title:
  The project deals with Analysis, Design and Implementation of Microcontroller based Very Low Variable Frequency Inverter.

 ► Objectives:
  The project is driven by a set of objectives which are as follows:
  • Design of a microcontroller based 3-phase power inverter configuration.
  • Simulation of the selected power inverter configuration using PSPICE based on above design.
  • Implementation in hardware for practical use.
  • Reduce the cost of overall application.

 ► Organization of Thesis:
  • Chapter-1 deals with the introduction and overall view of the circuitry and components emphasized in the project.
  • Chapter-2 deals with the primary power converter, the 3-phase diode bridge, its analysis and selection of appropriate diode ratings based on the design.
  • Chapter-3 deals with the complete analysis, waveforms and design of DC-Link capacitor and inductor.
  • Chapter-4 deals with the operation, analysis of waveforms, switching sequences and design of MOSFET 3-phase bridge inverter configuration and selection of suitable devices based on the design.
  • Chapter-5 deals with the microcontroller AT89C52, its registers, block diagrams and programming to generate the required pulses.
  • Chapter-6 deals with the driver IR2110 IC, its function, interface circuit design, design considerations and exact SPICE model used for simulation.
  • Chapter-7 deals with Hardware implementations such as the 5V and 12V power supplies, driver circuits, diode bridges, inverter circuit and filter circuitry and simulation programs, schematics and results.
  • Chapter-8 deals with conclusion part of the project and scope of future work.
  • Suitable appendices and bibliography to follow.
Literature survey:
- The basic idea of the project has been taken from the paper presented at International conference on Electrical Energy Systems and Power Electronics in Emerging Economies.
- Most of the concepts of the project related to power circuit were referred from the book “Handbook of Power Electronics” By M.H.Rashid and the textbook “Power Electronics – Circuits, Devices and Applications “by M.H.Rashid.
- All the concepts related to microcontroller and its programming and hardware interface circuits are taken from the textbook “The 8051 Microcontroller” By Mazidi.
- The driver design, Spice model were implemented by referring to the website www.irf.com
- Apart from the above, textbooks such as O.P.Arora, Vedam Subhramanyam, Robert W Erickson and P.S.Bimbhra have also been referred in the development of thesis.

Simplified Block Diagram:

Fig 1.1: Basic Block Diagram of the hardware
- The diode bridge is fed from a 3-phase ac supply mains through a 3-ph auto transformer. The diode bridge gives DC voltage with ripple content in it.
- The ripples in voltage and the input current in the DC Link are smoothened out by a properly designed DC link filter which is usually an LC filter. In addition this task the filter also eliminates certain harmonics present thereby improving the overall quality of the DC supply.
- The 3-phase MOSFET bridge inverter configuration is fed from the filter output.
The control circuit mainly comprises of the microcontroller interfaced to the frequency selector switch pad at its input port followed by the drivers at the output port.

The microcontroller is programmed to obtain the gating sequences in accordance to the frequency selected by the frequency selector switch pad.

The driver ics along with its designed interface circuit is fed from the microcontroller’s output port drives the Mosfet Bridge in accordance with the program dumped in the microcontroller with the help of programmer kit.

The output is fed to a three phase load weather R or RL load.

In order to facilitate better utilization of Mosfets and to obtain maximum output the inverter bridge is operated in 180° conduction mode.

**Hardware components:**

The hardware circuit has been implemented using the following devices:

- Diode bridge has been implemented using stud mounted type .5A,450V diodes
- DC Link filter has been implemented using ferrite cored wound 47mH inductor and 1000µF,105°C, ultra ripple capacitors.
- The inverter bridge configuration has been implemented using IRF840 power MOSFETs with suitable heat sinks.
- Frequency selector switch pads have been implemented with simple SPST switches.
- Power supplies for ics have been implemented using L7805 and L7812 regulator ics apart from a 12-0-12 transformer.
- The microcontroller used was Atmel AT89C52 programmed in an 8051 programmer kit.
- The driver ics IR2110 forms the heart of the circuit.

**Software components:**

- Programming of microcontroller was done in Keil software and was dumped into the controller with the help of Proload software.
- Simulation of simple circuits and discrete blocks of the main circuit was done in Multisim.
- Simulation of the entire power circuit along with design of DC-Link and estimation of total harmonic distortion (THD) and Fourier components of the outputs were done using PSPICE text editor.
- Schematics of the circuit were simulated using PSPICE Schematics.
- Simulation was done by considering exact models of Diodes (Dbreak), power MOSFET IRF840 sub circuit model and IR2110 SPICE model (full version of PSPICE only).
- AC sweep analysis was performed on DC-link capacitor currents so as to compensate any poles present in the right half of s-plane using PSPICE Schematics.
- Exact PWM inverter model was simulated in SIMULINK as a restudy to gain better understanding of the project.
Applications:

Applications of the variable very low frequency Inverters are as follows:

- Used as power supply for oscillating motors, as the stroke length in these motors varies as frequency of supply varies.
- The inverter also incorporates 400Hz frequency which is widely used actuators in space systems and International Space Station (ISS). Hence these systems are widely compatible with solar power.
- These supply systems are also widely employed in simulators and vibrating suspension test beds for heavy vehicles where a variety of frequencies are used to simulate the actual conditions.
CHAPTER 2

3- PHASE UNCONTROLLED DIODE BRIDGE RECTIFIER

Introduction:
- The three phase diode bridge employed is the primary power converter employed to convert the 3-ph ac supply to pulsating DC-supply.
- It is commonly used in high power applications and is a full rectifier.
- It can operate with or without a transformer and is a six pulse rectifier with overall improved conversion efficiency of 99.83% over its single phase counterpart.
- At any instant the pair of diodes which have the highest amount of instantaneous line-line voltage will conduct.
- Each diode in the three phase bridge conducts for duration of 120°.

Analysis:
- Fourier analysis of line voltages and supply side currents is essential to estimate the values of DC-Link components and filters to be employed.
- If \( V_m \) is the peak value of phase voltage then the instantaneous value of the supply phase voltages are given by:
  \[ V_{an} = V_m \sin(\omega t), \quad V_{bn} = V_m \sin(\omega t - 120^\circ), \quad V_{cn} = V_m \sin(\omega t - 240^\circ) \]
- Since the line to line voltages lead the phase values by 30°, the instantaneous line voltages are given by:
  \[ V_{ab} = \sqrt{3}V_m \sin(\omega t + 30^\circ), \quad V_{bc} = \sqrt{3}V_m \sin(\omega t - 90^\circ) \]
  \[ \text{And } V_{ca} = \sqrt{3}V_m \sin(\omega t - 210^\circ). \]
- The average value of output voltage is given by:
  \[ V_{dc} = \frac{2}{\pi} \int_0^\pi \sqrt{3}V_m \cos(\omega t) d(\omega t) = \frac{3\sqrt{3}}{\pi} V_m \]
- From the Fourier series of a q-pulse rectifier:
  \[ v_0(t) = V_m \frac{q}{\pi} \sin\frac{\pi}{q} \left(1 - \sum_{n=q,2q,4q,...}^{\infty} \frac{2}{n^2 - 1} \cos\frac{n\pi}{q} \cos n\omega t\right) \]
- For a three phase rectifier \( q=6 \) and thus the instantaneous output voltage of the rectifier is given as:
  \[ V_0(t) = 0.9549V_m \left[1 + \frac{2}{35} \cos 6\omega t - \frac{2}{143} \cos 12\omega t + \ldots \right] \]
- From the above analysis it is clear that the output voltage of the bridge rectifier contains only even harmonics with the sixth harmonic being the dominant one. Hence the filter design should be such that sixth and twelfth harmonics are eliminated from the output DC voltage.
Rectifier circuit Design:

- The design criteria of rectifier involve determining the ratings of semiconductor diodes.
- The ratings that are normally specified are average current, RMS current, Peak current and peak inverse voltage across the diode.
- The above mentioned criterion depends upon the load and circuit operating conditions. Since R load is easy for analysis and design part and the hardware has been designed for both R and RL loads analysis of RL load is done with PSPICE.

![PIV voltages using PSPICE](image-url)
Thus from the power diodes of appropriate ratings have been selected in accordance with the above obtained values.
CHAPTER 3

ANALYSIS AND DESIGN OF DC LINK FILTER

Introduction:
- It is the duty of a rectifier to provide an output voltage that should be as smooth as possible which is not possible in practical cases. So 3-phase six pulse rectifiers are preferred.
- However with the above configuration also considerable ac components of voltage and currents are present i.e. harmonics which does no useful work.
- These components must be filtered out and the ripples must be smoothened in order to obtain output as close as possible to pure DC value. Hence a DC link filter is employed to perform this task.
- In addition to above two functions a DC link filter feeding an inverter should also be capable of storing the entire power being fed to load momentarily.

Types of DC Link filters:
- An LC-Filter was preferred because of its simplicity in design and satisfactory performance.
- The inductor blocks the dominant harmonics and smoothes out ripples in current. Capacitor provides easy path to harmonics and smoothes out the ripple in voltage.

Design of Capacitor in DC-Link filter:
- In design of the DC-Link capacitor few operating conditions have to be selected first. They are as follows:
  1. Select the operating voltage of the capacitor
  2. Select the maximum desired ripple content in the DC-Link.
  3. Select the output power of the load to be supplied.
  4. A compromise between the above two conditions (2&3) is essential.
- Based on the above selected values the capacitor value can be obtained according to the relation
  \[ P_0 = C \frac{dV_c}{dt} * V \]
  where \( P_0 \) = Desired output power of the load to be supplied
supplied, \( C \) is the unknown capacitor value, \( V_C \) is the selected operating DC–Link voltage, \( dV_C \) is the peak-peak value of the desired ripple voltage in the DC-Link.

- Since 6\(^{th}\) harmonic is the dominant harmonic in the output of 3-ph bridge rectifier the value of \( C \) is also found out from the condition
\[
\frac{10}{n \omega C} \approx \sqrt{R_L^2 + (n \omega L_L)^2}
\]
where \( n \) is the harmonic number, \( C \) is the unknown Value of capacitor, \( R_L \) and \( L_L \) are load parameters and factor 10 is the safety condition.

- A compromise among the two conditions lead to the selection of a practical value of the capacitor with \( C_E = 880\mu F @ 2.16\% \) ripple, ESR value = 0.142 ohm at operating DC-Link voltage of about 200V.

- It is necessary to use a Series resistance i.e. Electrostatic Surge Resistance (ESR) with capacitor for modeling and simulation purposes to achieve converged solution.

#### Design of DC-Link Inductor:

- The operating conditions that have to be selected before commencing the design of dc-link inductor are as follows:
  1. Select the desired maximum load current
  2. Select the maximum desired ripple in DC-Link current.
  3. The harmonic component to be eliminated.

- The value of inductor can be calculated from the condition
\[
\frac{10}{n \omega L} \approx \sqrt{R_L^2 + (n \omega L_L)^2}
\]
Where \( n \) is the harmonic number, \( L \) is the unknown value of DC-Link inductor, \( R_L \) and \( L_L \) are the load parameters.

- The value of inductor is also calculated by writing the Fourier series of the input current of 3-ph diode bridge as:
\[
i(t) = a_0 + \sum_{n=1}^{\infty} (a_n \cos n\omega t + b_n \sin n\omega t)
\]
\[
a_0 = 0; \quad a_n = 0;
\]
\[
b_n = \frac{1}{n} \left[ \int_0^{\frac{\pi}{6}} I_a \cos n\omega t \, d(\omega t) - \int_{\frac{\pi}{6}}^{\frac{\pi}{2}} I_a \cos n\omega t \, d(\omega t) \right]
\]
\[
b_n = \frac{-4I_a}{n\pi} \cos n\pi \sin \frac{n\pi}{2} \sin \frac{n\pi}{3} \quad \text{for } n = 1, 5, 7, 11, 13, \ldots
\]
\[
b_n = 0 \quad \text{for } n = 2, 3, 4, 6, 8, 9, \ldots
\]

- Thus Fourier series of current is given by:
\[
i_s = \sum_{n=1}^{\infty} \frac{4\sqrt{3} I_a}{2\pi} \left( \sin(\omega t) \sin(5\omega t) \sin(7\omega t) \sin(11\omega t) + \sin(13\omega t) - \sin(17\omega t) - \ldots \right)
\]
Thus 5\(^{th}\) harmonic is the dominant one.

- By using the above condition
\[
\frac{10}{n \omega L} \approx \sqrt{R_L^2 + (n \omega L_L)^2}
\]
the value of inductor which eliminates 5\(^{th}\) harmonic must be calculated.

- Another condition which must be taken into account in calculation of DC-Link inductor value is the maximum permissible ripple value of current in DC-Link.
- The Fourier series of DC Link voltage is given by:
  \[ V_0(t) = 0.9549V_m [1 + \frac{2}{35}\cos 6\omega t - \frac{2}{143}\cos 12\omega t + \cdots \cdots \cdots] \]
  The dominant harmonic being 6th harmonic.
- Thus DC–Link current is given by:
  \[ i_0(t) = \frac{0.9549V_m}{\sqrt{R_L^2 + (\omega L)^2}} [1 + \frac{2}{35}\cos 6\omega t - \frac{2}{143}\cos 12\omega t + \cdots \cdots \cdots] \]
  Let \[ \frac{0.9549V_m}{\sqrt{R_L^2 + (\omega L)^2}} = I_{DC} \], then the RMS value of ripple current in DC link is:
  \[ I_{ripple} = I_{DC} \sqrt{\left(\frac{2}{35}\cos 6\omega t\right)^2 + \left(\frac{2}{143}\cos 12\omega t\right)^2} \]
  Where \( I_{ripple} \) is the desired value of current ripple in the DC link.
- From the above equation the value of DC-Link inductor is found out and a suitable practical value is selected.
- Compromises among the above conditions lead to the selection of a practical of 47mH

**Simulation results using Multisim and PSPICE:**

![Simulated test circuit of DC-Link filter using Multisim](image)

**Fig: 3.1 simulated test circuit of DC-Link filter using Multisim**
Fig 3.2 Simulation results showing reduced ripple content and harmonics in DC-Link

Fig 3.3: Simulation results showing ripple current through DC-Link inductor using PSPICE
Fig 3.4: Simulated results of Capacitor and Inductor current using designed values in PSPICE
CHAPTER 4
ANALYSIS AND DESIGN OF 3-PHASE MOSFET BRIDGE INVERTER

Introduction:
- Three phase inverters are generally used for high power applications
- A 3-ph output can be obtained by connecting six valves in bridge configuration.
- Two types of control signals can be applied to the valves: 180° conduction or 120° conduction. The 180° conduction method is preferred among the two since it has better utilization of valves.

Schematics of 3-ph MOSFET bridge:

180° Mode of conduction:
- In this mode of conduction each MOSFET conducts for 180° and three MOSFETs remain ON at any time.
- There are 6 modes of operation in each cycle and duration of each mode is 60°. The gating signal are shifted from each other by 60° to obtain balanced three phase voltages.
- Two switches of one leg cannot be switched ON simultaneously; this would result in direct short circuit of the DC supply voltage.
- Similarly 2 switches of any leg of the inverter cannot be switched off simultaneously as it would result in voltages that depend on respective line current polarity.
Switch states for 3-ph Voltage Source Inverter (VSI)

**state is 1 if two switches: 1 upper and 1 lower conduct such that output is \(+V_{DC}\) and 0 vice-versa.

<table>
<thead>
<tr>
<th>State</th>
<th>State no.</th>
<th>Switch States</th>
<th>(V_{ab})</th>
<th>(V_{bc})</th>
<th>(V_{ca})</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q1,Q2 and Q6 are ON ; Q4,Q5 and Q3 are OFF</td>
<td>1</td>
<td>100</td>
<td>(V_{DC})</td>
<td>0</td>
<td>(-V_{DC})</td>
</tr>
<tr>
<td>Q2,Q3 and Q1 are ON ; Q5,Q6 and Q4 are OFF</td>
<td>2</td>
<td>110</td>
<td>0</td>
<td>(V_{DC})</td>
<td>(-V_{DC})</td>
</tr>
<tr>
<td>Q3,Q4 and Q2 are ON ; Q6,Q1 and Q5 are OFF</td>
<td>3</td>
<td>010</td>
<td>(-V_{DC})</td>
<td>(V_{DC})</td>
<td>0</td>
</tr>
<tr>
<td>Q4,Q5 and Q3 are ON ; Q1,Q2 and Q6 are OFF</td>
<td>4</td>
<td>011</td>
<td>(-V_{DC})</td>
<td>0</td>
<td>(V_{DC})</td>
</tr>
<tr>
<td>Q5,Q6 and Q4 are ON ; Q2,Q3 and Q1 are OFF</td>
<td>5</td>
<td>001</td>
<td>0</td>
<td>(-V_{DC})</td>
<td>(V_{DC})</td>
</tr>
<tr>
<td>Q6,Q1 and Q5 are ON ; Q3,Q4 and Q2 are OFF</td>
<td>6</td>
<td>101</td>
<td>(V_{DC})</td>
<td>(-V_{DC})</td>
<td>0</td>
</tr>
<tr>
<td>Q1,Q3 and Q5 are ON ; Q4,Q6 and Q2 are OFF</td>
<td>7</td>
<td>111</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Q4,Q6 and Q2 are ON ; Q1,Q3 and Q5 are OFF</td>
<td>8</td>
<td>000</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

- States 7 and 8 produce zero line voltages and the line current free-wheels through the feedback diodes.
- To generate a given voltage waveform, the inverter moves from one state to another. The resulting ac output line voltages are built up of discrete values of voltages of \(V_{S},0,-V_{S}\). To generate the given waveform, the selection of states is done by a modulating technique that should assure the use of only valid states.

**Waveforms:**

![Waveform Diagram](image)

Fig 4.2: phase voltage output with R-load of 3-ph bridge inverter in Multisim
Fig 4.3: Output line voltage of a 3-ph Bridge inverter with R-Load

Fig 4.4: Load currents and voltages with RL-Load in PSPICE
Analysis of waveforms:
- Fourier analysis of the output voltage waveforms is done in order to obtain an estimate of the harmonic content and Harmonic distortion in the output variables.
- An estimate of ripple content in the DC-link current can be obtained by the analysis of output voltage and line currents.
- Fourier analysis of line and phase voltages:
  \[ V_{ab} = \frac{a_0}{2} + \sum_{n=1}^{\infty} (a_n \cos n\omega t + b_n \sin n\omega t) \]
  Due to quarter wave symmetry along x-axis, both \(a_0\) and \(a_n\) are zero. Assuming symmetry along y-axis at \(\omega t = \frac{\pi}{6}\) we can write:
  \[ b_n = \frac{1}{\pi} \left[ \int_{-\pi/6}^{\pi/6} -V_s d(\omega t) + \int_{5\pi/6}^{\pi} V_s d(\omega t) \right] \]
  Implies \(b_n = \frac{4V_s}{n\pi} \sin \left(\frac{n\pi}{2} \right) \sin \left(\frac{n\pi}{3} \right)\)
  Thus \(V_{ab} = \sum_{n=1,3,5,...}^{\infty} \frac{4V_s}{n\pi} \sin \left(\frac{n\pi}{3} \right) \sin n(\omega t + \frac{\pi}{6})\)
  Similarly \(V_{bc} = \sum_{n=1,3,5,...}^{\infty} \frac{4V_s}{n\pi} \sin \left(\frac{n\pi}{3} \right) \sin n(\omega t - \frac{\pi}{2})\)
  \(V_{ca} = \sum_{n=1,3,5,...}^{\infty} \frac{4V_s}{n\pi} \sin \left(\frac{n\pi}{3} \right) \sin n(\omega t - \frac{7\pi}{6})\)
- From the above equations it is clear that all the triplen harmonics \(n = 3, 9, 15, \ldots \) are eliminated from the line values of voltages.
- The RMS line-line voltage is given by \(V_L = \sqrt{\frac{1}{\pi} \int_{0}^{2\pi/3} V_s^2 d(\omega t)} = \sqrt{\frac{2}{3}} V_s = 0.8165 V_s\).
- For a star connected load the phase voltage is
  \(V_{an} = \sum_{n=1,3,5,...}^{\infty} \frac{4V_s}{\sqrt{3}n\pi} \sin \left(\frac{n\pi}{3} \right) \sin n(\omega t)\)
  Similarly \(V_{bn} = \sum_{n=1,3,5,...}^{\infty} \frac{4V_s}{\sqrt{3}n\pi} \sin \left(\frac{n\pi}{3} \right) \sin n(\omega t - \frac{2\pi}{3})\)
  \(V_{cn} = \sum_{n=1,3,5,...}^{\infty} \frac{4V_s}{\sqrt{3}n\pi} \sin \left(\frac{n\pi}{3} \right) \sin n(\omega t - \frac{4\pi}{3})\)
- The line current for RL load is given by
  \(i_a = \sum_{n=1,3,5,...}^{\infty} \frac{4V_s}{\sqrt{3}n\pi \sqrt{R^2 + (n\omega L)^2}} \sin \left(\frac{n\pi}{3} \right) \sin(n\omega t - \theta_n)\)
  Where \(\theta_n = \tan^{-1}\frac{n\omega L}{R}\)
- If load voltages are harmonic free, the DC supply current becomes harmonic free. However, because the load line voltages contain harmonics the DC supply current also contain harmonics.
Gating sequences of MOSFETS:
- Three square-wave gating signals $V_{g1}$, $V_{g3}$ and $V_{g5}$ at an output frequency $f_0$ and at 50% duty cycle. Signals $V_{g4}$, $V_{g6}$ and $V_{g2}$ should be logic invert signals of $V_{g1}$, $V_{g3}$ and $V_{g5}$ respectively. Each signal is shifted from each other by $60^\circ$.
- Signals $V_{g1}$, $V_{g3}$ and $V_{g5}$ drive Q1, Q3 and Q5 respectively, through gate isolating circuits. Signals $V_{g2}$, $V_{g4}$ and $V_{g6}$ can drive Q2, Q4 and Q6 respectively, without any isolating circuits.

Design and selection of MOSFETS:
- Design of an inverter comprises of determining the maximum current through the device, maximum load voltage and peak power to be supplied to the load.
- In addition to the above factors the operating frequency of the circuit, peak repetitive surge voltages and currents that the device may be subjected to during the operation of the circuit also determines the selection of the switch.
- The hardware circuit has been implemented using IRF840 Power MOSFET with max $V_{DSS}$ of 500V and max current of 8.0 A. More details can be obtained from the datasheet in Appendix.

Fig 4.5: currents through each Mosfet peak value = 1.6A
SPICE model for IRF840:

```
IRF-840 SUBCKT

xQ1 D G S IRF840 *subckt call for irf840*

.SUBCKT IRF840 1 2 3
M1 9 7 8 8 MM L=100u W=100u
.MODEL MM NMOS LEVEL=1 IS=1e-32
+VTO=3.84925 LAMBDA=0.00279225 KP=6.49028
+CGSO=1.18936e-05 CGDO=1e-11
RS 8 3 0.0178672
D1 3 1 MD
.MODEL MD D IS=6.51041e-09 RS=0.0106265 N=1.49911 BV=500
+IBV=0.00025 EG=1.2 XTI=3.02565 TT=0.0001
+CJO=1.08072e-09 VJ=3.67483 M=0.9 FC=0.5
RDS 3 1 2e+07
RD 9 1 0.810848
RG 2 7 3.45326
D2 4 5 MD1
.MODEL MD1 D IS=1e-32 N=50
+CJO=1.81945e-09 VJ=1.07167 M=0.9 FC=1e-08
D3 0 5 MD2
.MODEL MD2 D IS=1e-10 N=1 RS=3e-06
RL 5 10 1
FI2 7 9 VFI2 -1
VFI2 4 0 0
EV16 10 0 9 7 1
CAP 11 10 1.81945e-09
FI1 7 9 VFI1 -1
VFI1 11 6 0
RCAP 6 10 1
D4 0 6 MD3
.MODEL MD3 D IS=1e-10 N=1
.ENDS
```
CHAPTER 5
MICROCONTROLLER AT89C52 AND ITS PROGRAMMING

Features:

- 8K Bytes of In-System Reprogrammable Flash Memory
- Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-level Program Memory Lock
- 256 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-bit Timer/Counters
- Eight Interrupt Sources
- Programmable Serial Channel
- Low-power Idle and Power-down Modes

Absolute Maximum Ratings:

- Operating Temperature: -55°C to +125°C
- Storage Temperature: -65°C to +150°C
- Voltage on Any Pin with Respect to Ground: -1.0V to +7.0V
- Maximum Operating Voltage: 6.6V
- DC Output Current: 15.0 mA

Description:

- The AT89C52 is a low-power, high-performance CMOS 8-bit microcomputer with 8K bytes of Flash programmable and erasable read only memory (PEROM).
- The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer.
- The AT89C52 provides the following standard features: 8K bytes of Flash, 256 bytes of RAM, 32 I/O lines, three 16-bit timer/counters, a six-vector two-level interrupt architecture, a full-duplex serial port, on-chip oscillator, and clock circuitry.
- In addition, the AT89C52 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next hardware reset.
**Pin configuration:**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VCC</td>
</tr>
<tr>
<td>2</td>
<td>Port 1.0</td>
</tr>
<tr>
<td>3</td>
<td>Port 1.1</td>
</tr>
<tr>
<td>4</td>
<td>Port 1.2</td>
</tr>
<tr>
<td>5</td>
<td>Port 1.3</td>
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<tr>
<td>14</td>
<td>Port 1.12</td>
</tr>
<tr>
<td>15</td>
<td>Port 1.13</td>
</tr>
<tr>
<td>16</td>
<td>Port 1.14</td>
</tr>
<tr>
<td>17</td>
<td>Port 1.15</td>
</tr>
<tr>
<td>18</td>
<td>Port 1.16</td>
</tr>
<tr>
<td>19</td>
<td>Port 1.17</td>
</tr>
<tr>
<td>20</td>
<td>Port 1.18</td>
</tr>
</tbody>
</table>

**Pin Description:**

- **VCC**
  
  Supply voltage.

- **GND**
  
  Ground.

- **Port 0**
  
  Port 0 is an 8-bit open drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high impedance inputs. Port 0 can also be configured to be the multiplexed low order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups. Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pull-ups are required during program verification.

- **Port 1**
  
  Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that
are externally being pulled low will source current (IIL) because of the internal pullups. In addition, P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively, as shown in the following table. Port 1 also receives the low-order address bytes during Flash programming and verification.

<table>
<thead>
<tr>
<th>Port Pin</th>
<th>Alternate Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1.0</td>
<td>T2 (external count input to Timer/Counter 2), clock-out</td>
</tr>
<tr>
<td>P1.1</td>
<td>T2EX (Timer/Counter 2 capture/reload trigger and direction control)</td>
</tr>
</tbody>
</table>

- **Port 2**

  Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (IIL) because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that uses 8-bit addresses (MOVX @ RI); Port 2 emits the contents of the P2 Special Function Register. Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

- **Port 3**

  Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (IIL) because of the pull-ups. Port 3 also serves the functions of various special features of the AT89C51, as shown in the following table. Port 3 also receives some control signals for Flash programming and verification.

<table>
<thead>
<tr>
<th>Port Pin</th>
<th>Alternate Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>P3.0</td>
<td>RXD (serial input port)</td>
</tr>
<tr>
<td>P3.1</td>
<td>TXD (serial output port)</td>
</tr>
<tr>
<td>P3.2</td>
<td>INT0 (external interrupt 0)</td>
</tr>
<tr>
<td>P3.3</td>
<td>INT1 (external interrupt 1)</td>
</tr>
<tr>
<td>P3.4</td>
<td>T0 (timer 0 external input)</td>
</tr>
<tr>
<td>P3.5</td>
<td>T1 (timer 1 external input)</td>
</tr>
<tr>
<td>P3.6</td>
<td>WR (external data memory write strobe)</td>
</tr>
<tr>
<td>P3.7</td>
<td>RD (external data memory read strobe)</td>
</tr>
</tbody>
</table>
- **RST**
  Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

- **ALE/PROG**
  - Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory. If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

- **PSEN**
  Program Store Enable is the read strobe to external program memory. When the AT89C52 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

- **EA/VPP**
  External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset. EA should be strapped to VCC for internal program executions. This pin also receives the 12-volt programming enable voltage (VPP) during Flash programming when 12-volt programming is selected.

- **XTAL1**
  Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

- **XTAL2**
  Output from the inverting oscillator amplifier.
Block Diagram:
**Programming logic for the generation of gate pulses:**

```assembly
main:    setb fet1
        setb fet5
        setb fet6
        call delay
        clr fet5
        setb fet2
        call delay
        clr fet6
        setb fet3
        call delay
        clr fet1
        setb fet4
        call delay
        clr fet2
        setb fet5
        call delay
        clr fet3
        setb fet6
        call delay
        clr fet4
        jmp prog

delay:   mov A,r3
         mov r2,A
         mov a,r1

back:    mov r0,a
        here: djnz r0,here
        djnz r2,back
        ret
```
Avoid Damaging the port, an important precaution:

- We must be very careful when connecting a switch to an input port of 8051. This is due to the fact that wrong kind of connection can damage the port.
- “If a switch with $V_{CC}$ and ground is connected directly to the pin and M1 transistor is ON it will sink large currents from both internal load and the external $V_{CC}$. This can be too much current for M1, which will blow the transistor and damage the port bit.”
- PREVENTION: Certain precautions have to be followed to prevent the above damage. They are:
  1. One way is to have a 10K-ohm resistor on the $V_{CC}$ path to limit current flow through M1 transistor.
  2. Usage of a switch with ground only, and no $V_{CC}$. In this method, we read a low when the switch is pressed and we read a high when it is released.
  3. Another way is to connect any input switch to 74LS244 tristate buffer before it is fed to 8051 pin.
  4. Usage of right instructions when we want to read the status of the input pin.

These points are extremely important and must be emphasized since many people damage the ports and wonder how it happened without them.
CHAPTER 6

HIGH AND LOW SIDE MOSFET DRIVER

What is a driver:
- A gate driver is a circuit which provides necessary charge to turn on the power device apart from providing isolation and incorporating some protection features.

Necessity of a driver:
- The gating circuit is an integral part of a power converter that consists of power semiconductor devices. The output of a converter that depends upon how the gating circuit drives the switching devices is a direct function of switching.

MOSFET gate drive:
- Mosfets are voltage controlled devices and have very high input impedance. The gate draws a very small leakage current in order of nanoamperes.
- The turn-on time of the MOSFET depends upon the charging time of the input or gate capacitance.

Requirements of a MOSFET gate drive:
- To achieve switching speeds of 100ns or less the gate drive circuit should have a low output impedance and ability to sink relatively large currents. A totem pole configuration is capable of doing so.
- Gate voltage must be 10 to 15V higher than the source or emitter voltage because the power drive is connected to main high voltage rail +V_S, the gate voltage must be higher than the rail voltage.
- The gate voltage that is normally referred to ground must be controllable from the logic circuit. Thus control signals have to be level shifted to source terminal of the power device which in most applications swings between two rails V+.
- The power absorbed by the gate drive circuitry should be as low as possible and it should not significantly affect the overall efficiency of the power converter.

Gate driver functions:
- To provide sufficient gate charge to turn on the device (charge pump).
- Sensing of some overload conditions in power devices and appropriate counter measure taken in output buffer as well as fault status feedback.
Block diagram and description of IR2110:

- The input logic channels are controlled by TTL/CMOS compatible inputs such as port-1 of AT89C52 CMOS microcontroller.
- The transition threshold is proportional to logic supply $V_{DD}$ (3.3 to 20V) and Schmitt trigger buffer with hysteresis equal to 105 OF $V_{DD}$ to accept inputs with long rise times.
- The IR2110 features two gate drive channels, hence independent input commands or single input command with complementary drive and a predetermined dead time of 10ns.
- The low side output side is implemented with two N-channel MOSFETs in totem pole configuration which acts as a current buffer and is capable of sinking and sourcing relatively larger currents.
- The source of the lower driver is independently brought out to pin-2 i.e. COM, so that direct connection can be made to the source of the power device for return of the gate drive current. This prevents either channel from operating under voltage lockout if $V_{CC}$ is below specified value.
- The high side channel has been built into an “isolation tub” capable of floating with respect to COM. The floating voltage is provided at the output by the level shifter circuit. This is done in order to restrict the gate to source voltage of the high side MOSFET within the maximum permissible limits.
- The tub floats at $V_{S}$ potential which is established by the applied voltage $V_{CC}$ (15V) and swings between the two rails.
- The gate charge for the high side MOSFET is provided by the bootstrap capacitor $C_{BOOT}$, which is charged by the $V_{CC}$ supply through the bootstrap diode $D_{BOOT}$ during the time when the power device is off.
- To prevent quick leakage of charge through the diode during MOSFET turn on the diode $D_{BOOT}$ should be a fast recovery diode of reverse recovery time < 100ns or less.
Since the capacitor is charged from a low voltage source $V_{CC}$, the power consumed by the gate drive circuit is small.

Further the UV detect filter eliminates unwanted noise in the input signal and the latch prevents glitches that are highly prone to occur due to fast switching.

### Logic table for IR2110:

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>SD</td>
<td>HIN</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
</tr>
</tbody>
</table>

### Logic waveforms:

![Figure 1. Input/Output Timing Diagram](image-url)
IR2110 interface circuit design:

Design conditions:

- $C_{VCC} >> C_{BOOFT}$
- $C_{BOOFT} >> C_{FET}$
- $C_{FET} = Q_G/V_{GS}$
- $I_{AVG} = Q_{GD} + Q_{GS}/t_{sw}$
- $R_{TOT} = V_{CC} - V_{GS}/I_{AVG}$
- $R_{TOT} = R_{DRP} + R_{GON}$
- $R_{DRP} = 7\ \text{Ohm}(\text{from driver datasheet})$
- $R_{TOT} - R_{DRP} = R_{GON}$
From the above tabulated conditions the interface circuit is designed and the designed values are as follows:

<table>
<thead>
<tr>
<th>Designed values:</th>
</tr>
</thead>
<tbody>
<tr>
<td>• ( D_{\text{BOOT}} ) MUR420 (fast recovery diode)</td>
</tr>
<tr>
<td>• 20V Zener diode</td>
</tr>
<tr>
<td>• ( C_{\text{VCC}} = 100\mu\text{F}, 200\text{V} )</td>
</tr>
<tr>
<td>• ( C_{\text{BOOT}} = 10\mu\text{F}, 65\text{V} )</td>
</tr>
<tr>
<td>• ( C_{\text{FET}} = 6.3\text{nF} )</td>
</tr>
<tr>
<td>• ( R_{\text{GON}} = 42.2\text{ Ohms} )</td>
</tr>
</tbody>
</table>

**Design considerations about Bootstrap circuit:**

- **Voltage ripple:** Three different situations can occur in the bootstrap capacitor charging. \( I_{\text{LOAD}} < 0 \); the load current flows in the low side MOSFET displaying relevant \( V_{\text{CEon}} \). \( V_{\text{BS}} = V_{\text{CC}} - V_{\text{F}} - V_{\text{CEon}} \) In this case we have the lowest value for \( V_{\text{BS}} \). This represents the worst case for the bootstrap Capacitor sizing. When the MOSFET is turned off the \( V_{\text{s}} \) node is pushed up by the load current until the high side freewheeling diode get forward biased.

- **Bootstrap Resistor:** A resistor \( (R_{\text{boot}}) \) is placed in series with bootstrap diode so as to limit the current when the bootstrap capacitor is initially charged. The choice of bootstrap resistor is strictly related to \( V_{\text{BS}} \) time-constant. The minimum on time for charging the bootstrap capacitor or for refreshing its charge must be verified against this time-constant.

- **Bootstrap Capacitor:** For high \( T_{\text{HON}} \) designs where is used an electrolytic tank capacitor, its ESR must be considered. This parasitic resistance forms a voltage divider with \( R_{\text{boot}} \) generating a voltage step on \( V_{\text{BS}} \) at the first charge of bootstrap capacitor. The voltage step and the related speed \( (dV_{\text{BS}}/dt) \) should be limited. As a general rule, ESR should meet the following constraint: \( \frac{\text{ESR}}{\text{ESR} + R_{\text{BOOT}}} \cdot V_{\text{CC}} \leq 3\text{V} \).

Parallel combination of small ceramic and large electrolytic capacitors is normally the best compromise, the first acting as fast charge tank for the gate charge only and limiting the \( dV_{\text{BS}}/dt \) by reducing the equivalent resistance, while the second keeps the \( V_{\text{BS}} \) voltage drop inside the desired \( \Delta V_{\text{BS}} \).

- **Bootstrap Diode:** The diode must have a \( BV > DC+ \) and a fast recovery time \( (trr < 100 \text{ ns}) \) to minimize the amount of charge fed back from the bootstrap capacitor to VCC supply.
- Zener Diode: A Zener diode can be used for gate protection of the MOSFET against over voltages caused by stray inductances which lower the voltage of COM beyond zero by 
\[ L \frac{di}{dt} \] where L is the stray inductance.

► SPICE model for IR2110:

Sub circuit call:  xdriver1 VDD HIN SD LIN VSS HO VB VS VCC COM LO IR2110

.SUBCKT IR2110 VDD HIN SD LIN VSS HO VB VS VCC COM LO
+PARAMS:
  + T1=-40 T2=25 T3=125
  + V1=10 V2=15 V3=20
  + tonT1=90n tonT2=120n tonT3=170n
  + tonV1=140n tonV2=120n tonV3=100n
  + toffT1=77n toffT2=94n toffT3=130n
  + toffV1=115n toffV2=94n toffV3=75n
  + tonVdd1=125n tonVdd2=120n tonVdd3=115n
  + toffVdd1=113n toffVdd2=94n toffVdd3=72n

.MODEL diode25 d
+IS=1.0e-14 RS=0.01 N=1 EG=1.11
+XTI=3 BV=25 IBV=0.0001 CJO=0
+VJ=0.75 M=0.333 FC=0.5 TT=0
+KF=0 AF=1

.MODEL diode525 d
+IS=1.0e-14 RS=0.01 N=1 EG=1.11
+XTI=3 BV=525 IBV=0.0001 CJO=0
+VJ=0.75 M=0.333 FC=0.5 TT=0
+KF=0 AF=1

C_MD1_C2 VSS MD2_Nor3b_2 10p
C_MD1_C3 VSS MD2_Inv2_1 10p
C_MD1_C1 VSS MD2_Inv1_1 1n
D_MD1_D2 VSS HIN diode25
D_MD1_D3 SD VDD diode25
D_MD1_D4 VSS SD diode25
D_MD1_D5 LIN VDD diode25
D_MD1_D6 VSS LIN diode25
D_MD1_D7 VSS VDD diode25
D_MD1_D1 HIN VDD diode25
C_MD1_Trig3_CTrig VSS MD2_Inv2_1 10p
R_MD1_Trig3_R1Trig MD1_Trig3_3 VDD 100Meg
R_MD1_Trig3_R2Trig MD1_Trig3_4 MD1_Trig3_3 66.7Meg
<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_MD2_RS2_C3</td>
<td>VSS MD2_Nor3b_2 10p IC=0</td>
</tr>
<tr>
<td>C_MD2_RS2_C10</td>
<td>MD2_RS2_7 MD2_RS2_5 10p</td>
</tr>
<tr>
<td>C_MD2_RS2_C11</td>
<td>MD2_RS2_3 MD2_RS2_7 10p</td>
</tr>
<tr>
<td>C_MD2_RS2_C12</td>
<td>VSS MD2_RS2_3 10p</td>
</tr>
<tr>
<td>C_MD2_RS2_C9</td>
<td>VSS MD2_Nor3b_3 10p</td>
</tr>
<tr>
<td>C_MD2_RS2_C8</td>
<td>MD2_Nor3b_3 MD2_RS2_6 10p</td>
</tr>
<tr>
<td>C_MD2_RS2_C1</td>
<td>VSS MD2_Nor3b_3 10p IC=0</td>
</tr>
<tr>
<td>S_MD2_RS2_P1</td>
<td>MD2_RS2_5 MD2_RS2_6 MD2_Nor3b_1 VSS</td>
</tr>
<tr>
<td>_MD2_RS2_P1</td>
<td>MD2_Nor3b_1 VSS 1G</td>
</tr>
<tr>
<td>.MODEL _MD2_RS2_P1 VSWITCH</td>
<td>Roff=1e6 Ron=1m Voff=4.9V Von=0.1V</td>
</tr>
<tr>
<td>S_MD2_RS2_P2</td>
<td>MD2_RS2_6 MD2_Nor3b_3 MD2_RS2_3 VSS</td>
</tr>
<tr>
<td>_MD2_RS2_P2</td>
<td>MD2_RS2_3 VSS 1G</td>
</tr>
<tr>
<td>.MODEL _MD2_RS2_P2 VSWITCH</td>
<td>Roff=1e6 Ron=1m Voff=4.9V Von=0.1V</td>
</tr>
<tr>
<td>S_MD2_RS2_N1</td>
<td>MD2_Nor3b_3 VSS MD2_RS2_6 VSS _MD2_RS2_N1</td>
</tr>
<tr>
<td>RS_MD2_RS2_N1</td>
<td>MD2_RS2_3 VSS 1G</td>
</tr>
<tr>
<td>.MODEL _MD2_RS2_N1 VSWITCH</td>
<td>Roff=1e8 Ron=1m Voff=0.1V Von=4.9V</td>
</tr>
<tr>
<td>S_MD2_RS2_P3</td>
<td>MD2_RS2_5 MD2_RS2_6 MD2_Nor3b_2 VSS</td>
</tr>
<tr>
<td>_MD2_RS2_P3</td>
<td>MD2_RS2_3 VSS 1G</td>
</tr>
<tr>
<td>.MODEL _MD2_RS2_P3 VSWITCH</td>
<td>Roff=1e6 Ron=1m Voff=4.9V Von=0.1V</td>
</tr>
<tr>
<td>S_MD2_RS2_P4</td>
<td>MD2_RS2_7 MD2_RS2_3 MD2_Nor3b_3 VSS</td>
</tr>
<tr>
<td>_MD2_RS2_P4</td>
<td>MD2_RS2_3 VSS 1G</td>
</tr>
<tr>
<td>.MODEL _MD2_RS2_P4 VSWITCH</td>
<td>Roff=1e6 Ron=1m Voff=4.9V Von=0.1V</td>
</tr>
<tr>
<td>S_MD2_RS2_N3</td>
<td>MD2_RS2_3 VSS MD2_Nor3b_2 VSS _MD2_RS2_N3</td>
</tr>
<tr>
<td>RS_MD2_RS2_N3</td>
<td>MD2_Nor3b_2 VSS 1G</td>
</tr>
<tr>
<td>.MODEL _MD2_RS2_N3 VSWITCH</td>
<td>Roff=1e8 Ron=1m Voff=0.1V Von=4.9V</td>
</tr>
<tr>
<td>S_MD2_RS2_V1</td>
<td>MD2_RS2_5 VSS 5V</td>
</tr>
<tr>
<td>RS_MD2_RS2_N4</td>
<td>MD2_RS2_3 VSS MD2_Nor3b_3 VSS _MD2_RS2_N4</td>
</tr>
<tr>
<td>.MODEL _MD2_RS2_N4 VSWITCH</td>
<td>Roff=1e8 Ron=1m Voff=0.1V Von=4.9V</td>
</tr>
<tr>
<td>S_MD2_RS2_N2</td>
<td>MD2_Nor3b_3 VSS MD2_Nor3b_1 VSS _MD2_RS2_N2</td>
</tr>
<tr>
<td>RS_MD2_RS2_N2</td>
<td>MD2_Nor3b_1 VSS 1G</td>
</tr>
<tr>
<td>.MODEL _MD2_RS2_N2 VSWITCH</td>
<td>Roff=1e8 Ron=1m Voff=0.1V Von=4.9V</td>
</tr>
<tr>
<td>S_MD2_Nor3a_P1</td>
<td>MD2_Nor3a_4 MD2_Nor3a_5 MD2_Nor3a_1 VSS</td>
</tr>
<tr>
<td>_MD2_Nor3a_P1</td>
<td>MD2_Nor3a_1 VSS 1G</td>
</tr>
<tr>
<td>.MODEL _MD2_Nor3a_P1 VSWITCH</td>
<td>Roff=1e6 Ron=1 Voff=4.9V Von=0.1V</td>
</tr>
<tr>
<td>S_MD2_Nor3a_P2</td>
<td>MD2_Nor3a_5 MD2_Nor3a_6 MD2_Nor3b_2 VSS</td>
</tr>
<tr>
<td>_MD2_Nor3a_P2</td>
<td>MD2_Nor3b_2 VSS 1G</td>
</tr>
</tbody>
</table>
ANALYSIS, DESIGN AND IMPLEMENTATION OF MICROCONTROLLER BASED VARIABLE LOW FREQUENCY 3-PHASE POWER SUPPLY

```
.MMODEL  _MD2_Nor3a_P2 VSWITCH Roff=1e6 Ron=1 Voff=4.9V Von=0.1V
S_MD2_Nor3a_P3  MD2_Nor3a_6 MD3_DlyHS_2 MD2_Nor3a_3 VSS
_MD2_Nor3a_P3
RS_MD2_Nor3a_P3  MD2_Nor3a_3 VSS 1G

.MMODEL  _MD2_Nor3a_P3 VSWITCH Roff=1e6 Ron=1 Voff=4.9V Von=0.1V
S_MD2_Nor3a_N1  MD3_DlyHS_2 VSS MD2_Nor3b_2 VSS _MD2_Nor3a_N1
RS_MD2_Nor3a_N1  MD2_Nor3b_2 VSS 1G

.MMODEL  _MD2_Nor3a_N1 VSWITCH Roff=1e6 Ron=1 Voff=0.1V Von=4.9V
V_MD2_Nor3a_V  MD2_Nor3a_4 VSS 5V
S_MD2_Nor3a_N2  MD3_DlyHS_2 VSS MD2_Nor3a_1 VSS _MD2_Nor3a_N2
RS_MD2_Nor3a_N2  MD2_Nor3a_1 VSS 1G

.MMODEL  _MD2_Nor3a_N2 VSWITCH Roff=1e6 Ron=1 Voff=0.1V Von=4.9V
S_MD2_Nor3a_N3  MD3_DlyHS_2 VSS MD2_Nor3a_3 VSS _MD2_Nor3a_N3
RS_MD2_Nor3a_N3  MD2_Nor3a_3 VSS 1G

.MMODEL  _MD2_Nor3a_N3 VSWITCH Roff=1e6 Ron=1 Voff=0.1V Von=4.9V
S_MD2_Nor3b_P1 MD2_Nor3b_4 MD2_Nor3b_5 MD2_Nor3b_1 VSS
_MD2_Nor3b_P1
RS_MD2_Nor3b_P1  MD2_Nor3b_1 VSS 1G

.MMODEL  _MD2_Nor3b_P1 VSWITCH Roff=1e6 Ron=1 Voff=4.9V Von=0.1V
S_MD2_Nor3b_P2  MD2_Nor3b_5 MD2_Nor3b_6 MD2_Nor3b_2 VSS
_MD2_Nor3b_P2
RS_MD2_Nor3b_P2  MD2_Nor3b_2 VSS 1G

.MMODEL  _MD2_Nor3b_P2 VSWITCH Roff=1e6 Ron=1 Voff=4.9V Von=0.1V
S_MD2_Nor3b_P3  MD2_Nor3b_6 MD3_DlyLS_2 MD2_Nor3b_3 VSS
_MD2_Nor3b_P3
RS_MD2_Nor3b_P3  MD2_Nor3b_3 VSS 1G

.MMODEL  _MD2_Nor3b_P3 VSWITCH Roff=1e6 Ron=1 Voff=4.9V Von=0.1V
S_MD2_Nor3b_N1  MD3_DlyLS_2 VSS MD2_Nor3b_2 VSS _MD2_Nor3b_N1
RS_MD2_Nor3b_N1  MD2_Nor3b_2 VSS 1G

.MMODEL  _MD2_Nor3b_N1 VSWITCH Roff=1e6 Ron=1 Voff=0.1V Von=4.9V
V_MD2_Nor3b_V  MD2_Nor3b_4 VSS 5V
S_MD2_Nor3b_N2  MD3_DlyLS_2 VSS MD2_Nor3b_1 VSS _MD2_Nor3b_N2
RS_MD2_Nor3b_N2  MD2_Nor3b_1 VSS 1G

.MMODEL  _MD2_Nor3b_N2 VSWITCH Roff=1e6 Ron=1 Voff=0.1V Von=4.9V
S_MD2_Nor3b_N3  MD3_DlyLS_2 VSS MD2_Nor3b_3 VSS _MD2_Nor3b_N3
RS_MD2_Nor3b_N3  MD2_Nor3b_3 VSS 1G

.MMODEL  _MD2_Nor3b_N3 VSWITCH Roff=1e6 Ron=1 Voff=0.1V Von=4.9V
D_MD5_D2  com LO diode25
D_MD5_D1  LO VCC diode25
C_MD5_C  com LO 10p
C_MD5_Uvcc_c1 MD5_Uvcc_2 MD5_Uvcc_3 10n
C_MD5_Uvcc_c2 MD5_Uvcc_4 MD5_Uvcc_2 10n
C_MD5_Uvcc_c3 com MD4_Inv5_1 10p
```
```
E_MD5_Uvcc_ABM2 MD5_Uvcc_3 com VALUE { 8.3+(8.8-8.3)/(125+40)*(TEMP+40) } +
E_MD5_Uvcc_ABM3 MD5_Uvcc_4 com VALUE { 8.0+(8.5-8.0)/(125+40)*(TEMP+40) } +
X_MD5_Uvcc_Comp VCC MD5_Uvcc_2 MD4_Inv5_1 com COMP
S_MD5_Uvcc_P MD5_Uvcc_3 MD5_Uvcc_2 MD4_Inv5_1 com _MD5_Uvcc_P
RS_MD5_Uvcc_P MD4_Inv5_1 com 1G
.MODEL _MD5_Uvcc_P VSWITCH Roff=1e6 Ron=1 Voff=4.99 Von=0.01
S_MD5_Uvcc_N MD5_Uvcc_2 MD5_Uvcc_4 MD4_Inv5_1 com _MD5_Uvcc_N
RS_MD5_Uvcc_N MD4_Inv5_1 com 1G
.MODEL _MD5_Uvcc_N VSWITCH Roff=1e6 Ron=1 Voff=0.01 Von=4.99
S_MD5_Nand_P1 MD5_Nand_5 MD5_OLS_1 MD4_Inv5_1 VSS _MD5_Nand_P1
RS_MD5_Nand_P1 MD4_Inv5_1 VSS 1G
.MODEL _MD5_Nand_P1 VSWITCH Roff=1e6 Ron=1 Voff=4.9 Von=0.1
S_MD5_Nand_N1 MD5_OLS_1 MD5_Nand_4 MD3_DlyLS_8 VSS _MD5_Nand_N1
RS_MD5_Nand_N1 MD3_DlyLS_8 VSS 1G
.MODEL _MD5_Nand_N1 VSWITCH Roff=1e6 Ron=1 Voff=0.1 Von=4.9
S_MD5_Nand_P2 MD5_Nand_5 MD5_OLS_1 MD3_DlyLS_8 VSS _MD5_Nand_P2
RS_MD5_Nand_P2 MD3_DlyLS_8 VSS 1G
.MODEL _MD5_Nand_P2 VSWITCH Roff=1e6 Ron=1 Voff=4.9 Von=0.1
V_MD5_Nand_V MD5_Nand_5 VSS 5V
S_MD5_Nand_N2 MD5_Nand_4 VSS MD4_Inv5_1 VSS _MD5_Nand_N2
RS_MD5_Nand_N2 MD4_Inv5_1 VSS 1G
.MODEL _MD5_Nand_N2 VSWITCH Roff=1e6 Ron=1 Voff=0.1 Von=4.9
S_MD5_OLS_P VCC MD5_OLS_2 MD5_OLS_1 com _MD5_OLS_P
RS_MD5_OLS_P MD5_OLS_1 com 1G
.MODEL _MD5_OLS_P VSWITCH Roff=1e9 Ron=1m Voff=4.9 Von=0.1
S_MD5_OLS_N MD5_OLS_3 com MD5_OLS_1 com _MD5_OLS_N
RS_MD5_OLS_N MD5_OLS_1 com 1G
.MODEL _MD5_OLS_N VSWITCH Roff=1e9 Ron=1m Voff=0.1 Von=4.9
R_MD5_OLS_R6 LO MD5_OLS_2 11.4 TC=0.00190676, 9.3240e-07
R_MD5_OLS_R7 MD5_OLS_3 LO 7.76 TC=0.00241396, 2.331e-06
R_MD5_R com VCC 83.3k TC=-0.00358599, 0.0000124556
D_MD5_D3 com VCC diode25
D_MD4_D2 HO VB diode25
D_MD4_D1 VS VB diode25
D_MD4_D4 com VB diode525
```
D_MD4_D5    com VS diode525
D_MD4_D3    VS HO diode25
C_MD4_C3    VS HO 10p IC=0
C_MD4_Uvbs_c1 MD4_Uvbs_2 MD4_Uvbs_4 10n
C_MD4_Uvbs_c2 MD4_Uvbs_5 MD4_Uvbs_2 10n
C_MD4_Uvbs_c3 com MD4_Inv4_1 10p
E_MD4_Uvbs_ABM18 MD4_Uvbs_4 com VALUE {
+ V(VS)+8.4+(8.9-8.4)/(125+40)*(TEMP+40) }
E_MD4_Uvbs_ABM19 MD4_Uvbs_5 com VALUE {
+ V(VS)+8.0+(8.45-8.0)/(125+40)*(TEMP+40) }
X_MD4_Uvbs_Comp VB MD4_Uvbs_2 MD4_Inv4_1 com COMP
S_MD4_Uvbs_P MD4_Uvbs_4 MD4_Uvbs_2 MD4_Inv4_1 com
_MD4_Uvbs_P
RS_MD4_Uvbs_P MD4_Inv4_1 com 1G
.MODEL _MD4_Uvbs_P VSWITCH Roff=1e6 Ron=1 Voff=4.99 Von=0.01
S_MD4_Uvbs_N MD4_Uvbs_2 MD4_Uvbs_5 MD4_Inv4_1 com
_MD4_Uvbs_N
RS_MD4_Uvbs_N MD4_Inv4_1 com 1G
.MODEL _MD4_Uvbs_N VSWITCH Roff=1e6 Ron=1 Voff=0.01 Von=4.99
V_MD4_Inv3_V MD4_Inv3_2 VSS 5V
C_MD4_Inv3_C VSS MD4_OHS_1 1p
S_MD4_Inv3_P MD4_Inv3_2 MD4_OHS_1 MD4_RS_4 VSS _MD4_Inv3_P
RS_MD4_Inv3_P MD4_RS_4 VSS 1G
.MODEL _MD4_Inv3_P VSWITCH Roff=1e6 Ron=1 Voff=4.9V Von=0.1V
S_MD4_Inv3_N MD4_OHS_1 VSS MD4_RS_4 VSS _MD4_Inv3_N
RS_MD4_Inv3_N MD4_RS_4 VSS 1G
.MODEL _MD4_Inv3_N VSWITCH Roff=1e6 Ron=1 Voff=0.1V Von=4.9V
C_MD4_RS_C7 MD4_RS_6 MD4_RS_5 10p
C_MD4_RS_C2 VSS MD4_Inv2_3 10p IC=0
C_MD4_RS_C3 VSS MD3_DlyHS_8 10p IC=0
C_MD4_RS_C10 MD4_RS_7 MD4_RS_5 10p
C_MD4_RS_C11 MD4_RS_3 MD4_RS_7 10p
C_MD4_RS_C12 VSS MD4_RS_3 10p
C_MD4_RS_C9 VSS MD4_RS_4 10p
C_MD4_RS_C8 MD4_RS_4 MD4_RS_6 10p
C_MD4_RS_C1 VSS MD4_RS_4 10p IC=0
S_MD4_RS_P1 MD4_RS_5 MD4_RS_6 MD4_Inv2_3 VSS _MD4_RS_P1
RS_MD4_RS_P1 MD4_Inv2_3 VSS 1G
.MODEL _MD4_RS_P1 VSWITCH Roff=1e6 Ron=1m Voff=4.9V Von=0.1V
S_MD4_RS_P2 MD4_RS_6 MD4_RS_4 MD4_RS_3 VSS _MD4_RS_P2
RS_MD4_RS_P2 MD4_RS_3 VSS 1G
.MODEL _MD4_RS_P2 VSWITCH Roff=1e6 Ron=1m Voff=4.9V Von=0.1V
S_MD4_RS_N1 MD4_RS_4 VSS MD4_RS_3 VSS _MD4_RS_N1
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V_MD4_Nor1_V       MD4_Nor1_3 VSS 5V
S_MD4_Nor1_P1       MD4_Nor1_3 MD4_Nor1_4 MD4_Nor1_1 VSS
_MD4_Nor1_P1
RS_MD4_Nor1_P1      MD4_Nor1_1 VSS 1G
.MODEL       _MD4_Nor1_P1 VSWITCH Roff=1e6 Ron=1 Voff=4.9 Von=0.1
S_MD4_Nor1_P2       MD4_Nor1_4 MD4_Nor1_5 MD4_Inv6_3 VSS
_MD4_Nor1_P2
RS_MD4_Nor1_P2      MD4_Inv6_3 VSS 1G
.MODEL       _MD4_Nor1_P2 VSWITCH Roff=1e6 Ron=1 Voff=4.9 Von=0.1
S_MD4_Nor1_N1       MD4_Nor1_5 VSS MD4_Inv6_3 VSS _MD4_Nor1_N1
RS_MD4_Nor1_N1      MD4_Inv6_3 VSS 1G
.MODEL       _MD4_Nor1_N1 VSWITCH Roff=1e6 Ron=1 Voff=0.1 Von=4.9
S_MD4_Nor1_N2       MD4_Nor1_5 VSS MD4_Nor1_1 VSS _MD4_Nor1_N2
RS_MD4_Nor1_N2      MD4_Nor1_1 VSS 1G
.MODEL       _MD4_Nor1_N2 VSWITCH Roff=1e6 Ron=1 Voff=0.1 Von=4.9
V_MD4_Inv5_V       MD4_Inv5_2 VSS 5V
C_MD4_Inv5_C       VSS MD4_Nor2_1 1p
S_MD4_Inv5_P       MD4_Inv5_2 MD4_Nor2_1 MD4_Inv5_1 VSS _MD4_Inv5_P
RS_MD4_Inv5_P      MD4_Inv5_1 VSS 1G
.MODEL       _MD4_Inv5_P VSWITCH Roff=1e6 Ron=1 Voff=4.9 Von=0.1V
S_MD4_Inv5_N       MD4_Nor2_1 VSS MD4_Inv5_1 VSS _MD4_Inv5_N
RS_MD4_Inv5_N      MD4_Inv5_1 VSS 1G
.MODEL       _MD4_Inv5_N VSWITCH Roff=1e6 Ron=1 Voff=0.1V Von=4.9V
V_MD4_Nor2_V       MD4_Nor2_3 VSS 5V
S_MD4_Nor2_P1       MD4_Nor2_3 MD4_Nor2_4 MD4_Nor2_1 VSS
_M4_Nor2_P1
RS_MD4_Nor2_P1      MD4_Nor2_1 VSS 1G
.MODEL       _MD4_Nor2_P1 VSWITCH Roff=1e6 Ron=1 Voff=4.9 Von=0.1
S_MD4_Nor2_P2       MD4_Nor2_4 MD4_Inv6_1 MD4_Nor2_2 VSS
_MD4_Nor2_P2
RS_MD4_Nor2_P2      MD4_Nor2_2 VSS 1G
.MODEL       _MD4_Nor2_P2 VSWITCH Roff=1e6 Ron=1 Voff=4.9 Von=0.1
S_MD4_Nor2_N1       MD4_Inv6_1 VSS MD4_Nor2_2 VSS _MD4_Nor2_N1
RS_MD4_Nor2_N1      MD4_Nor2_2 VSS 1G
.MODEL       _MD4_Nor2_N1 VSWITCH Roff=1e6 Ron=1 Voff=0.1 Von=4.9
S_MD4_Nor2_N2       MD4_Inv6_1 VSS MD4_Nor2_1 VSS _MD4_Nor2_N2
RS_MD4_Nor2_N2      MD4_Nor2_1 VSS 1G
.MODEL       _MD4_Nor2_N2 VSWITCH Roff=1e6 Ron=1 Voff=0.1 Von=4.9
V_MD4_Inv6_V       MD4_Inv6_2 VSS 5V
C_MD4_Inv6_C       VSS MD4_Inv6_3 1p
S_MD4_Inv6_P       MD4_Inv6_2 MD4_Inv6_3 MD4_Inv6_1 VSS _MD4_Inv6_P
RS_MD4_Inv6_P      MD4_Inv6_1 VSS 1G
.MODEL       _MD4_Inv6_P VSWITCH Roff=1e6 Ron=1 Voff=4.9 Von=0.1V
### ANALYSIS, DESIGN AND IMPLEMENTATION OF MICROCONTROLLER BASED VARIABLE LOW FREQUENCY 3-PHASE POWER SUPPLY

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<tr>
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<td>MD3_DlyHS_2 VSS 1G</td>
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<td>MD3_DlyHS_2 VSS 1G</td>
</tr>
<tr>
<td>.MODEL</td>
<td>_MD3_DlyHS_delay_N VSWITCH Roff=1e6 Ron=10 Voff=0.01V Von=4.99V</td>
</tr>
<tr>
<td>S_MD3_DlyHS_P1</td>
<td>MD3_DlyHS_10 MD3_DlyHS_11 MD3_DlyHS_6 VSS _MD3_DlyHS_P1</td>
</tr>
<tr>
<td>RS_MD3_DlyHS_P1</td>
<td>MD3_DlyHS_6 VSS 1G</td>
</tr>
<tr>
<td>.MODEL</td>
<td>_MD3_DlyHS_P1 VSWITCH Roff=1e6 Ron=1 Voff=4.9V Von=0.1V</td>
</tr>
<tr>
<td>S_MD3_DlyHS_P2</td>
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</tr>
<tr>
<td>RS_MD3_DlyHS_P2</td>
<td>MD3_DlyHS_8 VSS 1G</td>
</tr>
<tr>
<td>.MODEL</td>
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</tr>
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<td>S_MD3_DlyHS_N1</td>
<td>MD3_DlyHS_9 VSS MD3_DlyHS_8 VSS _MD3_DlyHS_N1</td>
</tr>
<tr>
<td>RS_MD3_DlyHS_N1</td>
<td>MD3_DlyHS_8 VSS 1G</td>
</tr>
<tr>
<td>.MODEL</td>
<td>_MD3_DlyHS_N1 VSWITCH Roff=1e6 Ron=1 Voff=0.1V Von=4.9V</td>
</tr>
<tr>
<td>S_MD3_DlyHS_MP1</td>
<td>MD3_DlyHS_12 MD3_DlyHS_13 MD3_DlyHS_9 VSS _MD3_DlyHS_MP1</td>
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<tr>
<td>RS_MD3_DlyHS_MP1</td>
<td>MD3_DlyHS_9 VSS 1G</td>
</tr>
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ANALYSIS, DESIGN AND IMPLEMENTATION OF MICROCONTROLLER BASED VARIABLE LOW FREQUENCY 3- PHASE POWER SUPPLY

\[
+ \{V1\}*(\{V2\}-\{V1\})/(10/10n))\}
\]

\[
V_{MD3\_DlyHS\_V\_delay} \quad MD3\_DlyHS\_20 \ VSS \ 5V
\]
\[
C_{MD3\_DlyHS\_C3} \quad VSS \ MD3\_DlyHS\_6 \ 10p
\]
\[
V_{MD3\_DlyHS\_VCC1} \quad MD3\_DlyHS\_10 \ VSS \ 5V
\]
\[
C_{MD3\_DlyHS\_C6} \quad VSS \ MD3\_DlyHS\_9 \ 10p \ IC=-5V
\]
\[
C_{MD3\_DlyHS\_C5} \quad VSS \ MD3\_DlyHS\_8 \ 10p \ IC=0V
\]
\[
V_{MD3\_DlyHS\_VCC2} \quad MD3\_DlyHS\_12 \ VSS \ 5V
\]
\[
S_{MD3\_DlyHS\_N2} \quad MD3\_DlyHS\_9 \ VSS \ MD3\_DlyHS\_6 \ VSS
\]
\[
\_MD3\_DlyHS\_N2
\]
\[
RS_{MD3\_DlyHS\_N2} \quad MD3\_DlyHS\_6 \ VSS \ 1G
\]
\[
\_MODEL \ _MD3\_DlyHS\_N2 \ VSWITCH \ Roff=1e6 \ Ron=1 \ Voff=0.1V \ Von=4.9V
\]
\[
C_{MD3\_DlyHS\_C4} \quad VSS \ MD3\_DlyHS\_7 \ 10p
\]
\[
E_{MD3\_DlyHS\_ABM13} \quad MD3\_DlyHS\_17 \ com \ VALUE \ \{\ (1-\exp(- (toffV1+((V3)-(V1))*((V(MD3\_DlyHS\_1))-(V1))/10/10n))/ + (1-\exp(- (toffV1+((V3)-(V1))*((V3)-(V1))/10/10n)) + \} \]
\[
C_{MD3\_DlyLS\_C} \quad VSS \ MD3\_DlyLS\_5 \ 10n
\]
\[
S_{MD3\_DlyLS\_delay\_P} \quad MD3\_DlyLS\_20 \ MD3\_DlyLS\_5 \ MD3\_DlyLS\_2 \ VSS
\]
\[
+_\_MD3\_DlyLS\_delay\_P
\]
\[
RS_{MD3\_DlyLS\_delay\_P} \quad MD3\_DlyLS\_2 \ VSS \ 1G
\]
\[
\_MODEL \ _MD3\_DlyLS\_delay\_P \ VSWITCH \ Roff=1e6 \ Ron=10 \ Voff=4.99V \ Von=0.01V
\]
\[
S_{MD3\_DlyLS\_delay\_N} \quad MD3\_DlyLS\_5 \ VSS \ MD3\_DlyLS\_2 \ VSS
\]
\[
+_\_MD3\_DlyLS\_delay\_N
\]
\[
RS_{MD3\_DlyLS\_delay\_N} \quad MD3\_DlyLS\_2 \ VSS \ 1G
\]
\[
\_MODEL \ _MD3\_DlyLS\_delay\_N \ VSWITCH \ Roff=1e6 \ Ron=10 \ Voff=0.01V \ Von=4.99V
\]
\[
S_{MD3\_DlyLS\_P1} \quad MD3\_DlyLS\_10 \ MD3\_DlyLS\_11 \ MD3\_DlyLS\_6 \ VSS
\]
\[
+_\_MD3\_DlyLS\_P1
\]
\[
RS_{MD3\_DlyLS\_P1} \quad MD3\_DlyLS\_6 \ VSS \ 1G
\]
\[
\_MODEL \ _MD3\_DlyLS\_P1 \ VSWITCH \ Roff=1e6 \ Ron=1 \ Voff=4.9V \ Von=0.1V
\]
\[
S_{MD3\_DlyLS\_P2} \quad MD3\_DlyLS\_11 \ MD3\_DlyLS\_9 \ MD3\_DlyLS\_8 \ VSS
\]
\[
+_\_MD3\_DlyLS\_P2
\]
\[
RS_{MD3\_DlyLS\_P2} \quad MD3\_DlyLS\_8 \ VSS \ 1G
\]
\[
\_MODEL \ _MD3\_DlyLS\_P2 \ VSWITCH \ Roff=1e6 \ Ron=1 \ Voff=4.9V \ Von=0.1V
\]
\[
S_{MD3\_DlyLS\_N1} \quad MD3\_DlyLS\_9 \ VSS \ MD3\_DlyLS\_8 \ VSS \ _MD3\_DlyLS\_N1
\]
\[
RS_{MD3\_DlyLS\_N1} \quad MD3\_DlyLS\_8 \ VSS \ 1G
\]
\[
\_MODEL \ _MD3\_DlyLS\_N1 \ VSWITCH \ Roff=1e6 \ Ron=1 \ Voff=0.1V \ Von=4.9V
\]
\[
S_{MD3\_DlyLS\_MP1} \quad MD3\_DlyLS\_12 \ MD3\_DlyLS\_13 \ MD3\_DlyLS\_9 \ VSS
\]
\[
+_\_MD3\_DlyLS\_MP1
\]
\[
RS_{MD3\_DlyLS\_MP1} \quad MD3\_DlyLS\_9 \ VSS \ 1G
V_MD3_DlyLS_V_delay MD3_DlyLS_20 VSS 5V
C_MD3_DlyLS_C3 VSS MD3_DlyLS_6 10p
V_MD3_DlyLS_VCC1 MD3_DlyLS_10 VSS 5V
C_MD3_DlyLS_C6 VSS MD3_DlyLS_9 10p IC=-5V
C_MD3_DlyLS_C5 VSS MD3_DlyLS_8 10p IC=0V
V_MD3_DlyLS_VCC2 MD3_DlyLS_12 VSS 5V
S_MD3_DlyLS_N2 MD3_DlyLS_9 VSS MD3_DlyLS_6 VSS _MD3_DlyLS_N2
RS_MD3_DlyLS_N2 MD3_DlyLS_6 VSS 1G
.MODEL _MD3_DlyLS_N2 VSWITCH Roff=1e6 Ron=1 Voff=0.1V Von=4.9V
C_MD3_DlyLS_C4 VSS MD3_DlyLS_7 10p
E_MD3_DlyLS_ABM13 MD3_DlyLS_17 com VALUE { (1-EXP(-
{toffV1}+({toffV3}-
V(VCC)-{V1}))/10/ 10n))
+ (1-EXP(- (toffV1)+(toffV3)-V2*(V3)-{V1}))/10/ 10n))
+ }
.ENDS IR2110
CHAPTER 7

HARDWARE IMPLEMENTATION AND SIMULATION RESULTS

► Hardware circuits implemented:
  • Common power supply for ICs +12V and +5V.
  • 3-phase Diode Bridge circuit along with DC-Link filters.
  • 3-phase Mosfet bridge Inverter circuit along with Driver Interface.
  • Microcontroller along with its interface and functional circuit
  • Frequency selection switch pad.

► Hardware components:

The hardware circuit has been implemented using the following devices:

  • Diode bridge has been implemented using stud mounted type 5A,450V diodes
  • DC Link filter has been implemented using ferrite cored wound 47mH inductor and 1000μF,105°C, ultra ripple capacitors.
  • The inverter bridge configuration has been implemented using IRF840 power MOSFETs with suitable heat sinks.
  • Frequency selector switch pads have been implemented with simple SPST switches.
  • Power supplies for ICs have been implemented using L7805 and L7812 regulator ICs apart from a 12-0-12 transformer.
  • The microcontroller used was Atmel AT89C52 programmed in an 8051 programmer kit.
  • The driver ICs IR2110 forms the heart of the circuit.

► Software components:

  • Programming of microcontroller was done in Keil software and was dumped into the controller with the help of Proload software.
  • Simulation of simple circuits and discrete blocks of the main circuit was done in Multisim.
  • Simulation of the entire power circuit along with design of DC-Link and estimation of total harmonic distortion (THD) and Fourier components of the outputs were done using PSPICE text editor.
  • Schematics of the circuit were simulated using PSPICE Schematics.
  • Simulation was done by considering exact models of Diodes (Dbreak), power MOSFET IRF840 sub circuit model and IR2110 SPICE model (full version of PSPICE only).
  • AC sweep analysis was performed on DC-link capacitor currents so as to compensate any poles present in the right half of s- plane using PSPICE Schematics.
  • Exact PWM inverter model was simulated in SIMULINK as a restudy to gain better understanding of the project.
Simulated circuits and results:

Fig 7.1: simulated power supply circuit +12V in Multisim

Fig 7.2: Simulation results for +12V power supply circuit

Fig 7.4: Simulated schematics for diode bridge along with filter using PSPICE

Schematics
Fig 7.5: Ripple voltage across filter capacitor - Simulation results using PSPICE

Fig 7.6: Ripple currents and voltage across DC-Link Inductor

DC-Link Inductor currents
Ripple currents 5% = 0.1359A
Fig 7.7 Schematics showing the power inverter along with driver IR2110

Fig 7.8 Schematics of single branch using PSPICE
Hardware design and Implementation of Regulated power supply:

- A “good” DC regulated power supply has always been the primary need of an electronic circuit designer. The requirements in the magnitudes of fixed DC voltage may differ from circuit but the stability, and regulation of power supply under varying loads with low cost will be important.

- The trend in voltage regulation is towards localized regulation with smaller, low cost, low current, fixed voltage IC regulators which require minimal heat sink and few or no external components. In the past one used bulky, high power regulators made up of any discrete components to regulate the line which supplied all areas of electronic system. Unfortunately the impedance of the line and associated connectors caused voltage drops which varied throughout the system. Also, any connector impedance in the line between chassis or cards could allow unwanted coupling between critical parts of the system. These older systems often required considerable by-passing or decoupling which caused degraded local regulation.

- The power supply standardization was thought of long with the development of various types pf integrated circuit (IC). These modern ICs were also designed with this in mind. The requirements for IC power supply has mainly converged to +5v. All TTLs or compatible chips use only +5v. However, there is yet another generation of CMOS chips or equal which may be operated on +12v. Operational, differential amplifiers and other industrial packages are commonly designed for +12v. The present day technology in regulator design emphasize low – current ranges and small low power three-lead
packages which are sufficient to supply the required power to these chips. These regulators are available in variety of positive and negative voltages at current ranges from 100mA to 5 amps. With this variety to choose it was possible to select the regulators for our applications and reduce cost significantly over compelling approaches.

**Design Aspects**: There are three primary factors which be fully described prior to the designing of filter and power supply. They are:

- the voltage
- the current
- the ripple requirements
- All the factors are dependent on the load requirement; therefore \( V_{\text{in}} \) and \( I_{\text{in}} \) in the following figure become a governing condition where:

\[
\begin{align*}
I_{\text{in}} &= I_{o} + I_{q} \quad \text{(Output current + regulator quiescent current.)} \\
I_{\text{in}} (\text{max}) &\approx I_{o} (\text{max}) \\
\text{Full load operating current} &\quad I_{\text{in}} (\text{min}) \leq I_{q} \\
\text{No load or minimum operating current} &\quad \text{could be near zero } V_{\text{in}} (pk) = V_{m} \\
\text{Maximum possible instantaneous no-load filter output voltage} &\quad \text{equal to peak value of transformer secondary voltage at highest design line voltage } V_{\text{pri}} \text{ limited by absolute maximum regulator input voltage.} \\
V_{\text{in}} &> V_{o} (V_{\text{in}} + 5 \text{ to } 10 \text{ volts}) \quad \text{(regulator dependent)} \\
\text{For power supplies using voltage regulators the filter will most often use capacitor input.} &\quad \text{Since these power supplies use only capacitive filters the discussion here is restricted to that only. The capacitive exhibit the following:}
\end{align*}
\]

1. Higher DC output voltage.
2. Higher peak to average diode forward current.
3. Lower diode PIV rating requirements.
4. Higher peak to average transformer currents.

- Poorer output voltage regulation with load variation and very high diode surge current at turn-on are few negative factors.
- The semiconductor diodes of moderate price meet most of the pear and surge requirements accept in supplies handling many amperes. Still it may be necessary to
balance increased diode and transformer cost against the alternative of a choke- input filter.

- In power supply designs employing voltage regulators, it is assumed that only moderate filter output regulation and ripple are required. A capacitor input filter would exhibit peak currents considerably lower. Ripple factor is inevitable as the capacitor discharges approximately linearly between voltage peaks.

► Working principle:
- Figure 7.1 shows the circuit diagram for power supply whereby IC78XX is used as positive regulator. The circuit consists of step down transformer which gives the ac input to the diode bridge, which will rectify the ac input thus generating ripples.
- The obtained ripples are passed through filters(C=1000microfarad) which will generate DC output. To stabilize the obtained DC output voltage it is passed through regulators as shown in the fig 7.9.

► HARDWARE IMPLEMENTATION:

Fig 7.10: Implemented Diode Bridges
Fig 7.11: Implemented DC-Link Filter

Fig 7.12: Implemented MOSFET Bridge Inverter
Fig 7.13: Microcontroller and its Interface

Fig 7.14: Implemented hardware circuitry of Driver and its interface to MOSFET Bridge
Fig. 7.15: Complete Circuitry
CHAPTER 8

CONCLUSION AND SCOPE OF FUTURE WORK

A summary of the major contributions of this work is presented in the following sections. The significance of the work and scope of future development based on this work has been included.

► **Summary of the present work:**
  - The major concern of developing an Inverter module for laboratory purposes has been overcome.
  - A 3-phase laboratory model of significant power level of 170W was developed and tested.
  - The above mentioned module has been thoroughly tested in simulation using Microsim and Multisim soft wares and the hardware was constructed.
  - The hardware was also tested and the practical results were found to be in complete agreement with that of the simulation results.

► **Contributions of present work:**
  - Design and analysis of a 3-phase inverter circuit has been accomplished.
  - Implementation of advanced microcontroller triggering has been achieved with a source code of little complexity.
  - Design of Interface circuitry for advanced driver Ics has been done leaving behind the conventional techniques.
  - Simulation using exact SPICE models for power Mosfets and driver ics was done.
  - Design of DC-link filter components has been emphasized.
  - Relatively larger power inverter of about 180W was developed in a very small kit with low expenditure.

► **Scope of Future work:**
  The extension of the present work can be done in following ways:
  - Output power levels can be extended up to 5kW by the use of suitable high power capacitors in DC-Link.
  - An additional power modulator stage i.e. a Buck-Boost chopper can be included with variable duty ratios ranging from 0.1 to 4.
  - More complex driver ics such as L6390ST and IR2137/2237 can be implemented.
  - Feedback paths from load can be provided using current sensing ics IR2175 and automatic over current protection can be realized.
  - Overvoltage protection of power inverters can be realized.
  - Advanced modulating techniques such as space-vector modulation can be employed.
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